Application/Control Number: 10/773,462

Art Unit: 2871

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to the <u>amended</u> claims 1 and 19 based on the Response filed on February 06, 2008 have been considered but are moot in view of the new ground(s) of rejection. Therefore, <u>this is Final action</u>.

Election/Restrictions

This application contains claims 3-4, 6-16, 18 and 20-32 drawn to an invention nonelected with traverse in the reply filed on July 30, 2007. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary sikl lin the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 5, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (US2001/0030722) in view of Makiko et al. (JP2000-122616) and Aoki et al. (US6177916B1).

Murade discloses (at least in Figs. 2-6) a liquid crystal display (LCD) panel comprising:

Claim 1:

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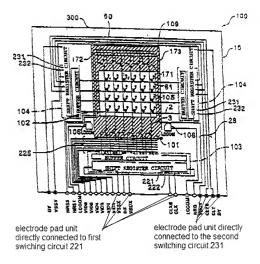
 a liquid crystal panel in which liquid crystal is 108 filled between upper 31 and lower 300 substrates and the liquid crystal is in communication with a display electrode (pixel electrode 14) and a common electrode (counter electrode 32) which face each other;

- a first driving circuit (shift register circuit 221) connected to the liquid crystal panel by a plurality of data lines and which applies a data signal to the liquid crystal panel;
- a second driving circuit (shift register circuit 231) connected to the liquid crystal panel by a plurality of gate lines and which applies a scan signal to sequentially apply the data signal to the liquid crystal panel;
- an electrode pad unit 107 which applies an alignment signal voltage to the liquid crystal panel for alignment of the liquid crystal filled in the liquid crystal panel;
- a first switching circuit (data sampling circuit 101) which performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the data lines

wherein

 the electrode pad unit is 107 directly connected to the first switching circuit and the second switching circuit as shown in Fig. 3: Application/Control Number: 10/773,462

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Claim 2:

 the first switching circuit 101 is placed between the first driving circuit 221 and the liquid crystal panel

Claim 5:

 the first buffer circuit 222 is placed between the first driving circuit and the first switching circuit 101.

Claim 19:

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 a liquid crystal panel comprising a plurality of pixels in liquid crystal to display images;

- a driving circuit supplying signals to the plurality of pixels to control the display images;
- an electrode unit to supply an alignment signal voltage to the liquid crystal panel;
 a switching circuit selectively switching the alignment signal voltage from the
 electrode unit to the liquid crystal display panel to align liquid crystal in the liquid crystal panel; and
- a buffer circuit connected to the driving circuit to prevent the alignment signal voltage from flowing to the driving circuit.

However, Murade fails to disclose a liquid crystal display (LCD) panel comprising:

- a second switching circuit which performs a switching operation to apply the
 alignment signal voltage applied via the electrode pad unit to the liquid crystal
 panel via the gate lines; where the second switching circuit is placed between the
 liquid crystal panel and the electrode pad unit (claim 17)
- first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits.

Makiko et al. teach (Fig. 1 and abstract) forming a liquid crystal display (LCD) panel comprising a second switching circuit 125, which performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the gate lines; where the second switching circuit is placed between

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the liquid crystal panel and the driving circuit 123; however, Murade discloses that the driving circuit is placed between the electrode pad and the liquid crystal panel, thus the second switching circuit is obviously placed between the liquid crystal panel and the electrode pad unit.

Aoki et al. teach (at least Fig. 1, col. 3, lines 51- col. 4, line 10) forming a liquid crystal display (LCD) panel comprising first and second buffer circuits 12, which prevent the alignment signal voltage from being applied to the first and second driving circuits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Murade disclosed with:

- (a) a second switching circuit that performs a switching operation to apply the alignment signal voltage applied via the electrode pad unit to the liquid crystal panel via the gate lines; where the second switching circuit is placed between the liquid crystal panel and the electrode pad unit for switching liquid crystal impressing voltage, as taught by Makiko (abstract);
- (b) first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits first and second buffer circuits, which prevent the alignment signal voltage from being applied to the first and second driving circuits for reducing parasistic capacitance loads thus improving the bandwidth characteristics of the bus lines even where the number of the bus lines increase, as taught by Aoki et al.

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Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julie-Huyen L. Ngo whose telephone number is (571) 272-2295. The examiner can normally be reached on M-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Julie-Huyen L. Ngo/ Primary Examiner Art Unit 2871